United International Journal of Engineering and Sciences
(UIJES – A Peer-Reviewed Journal); ISSN:2582-5887 | Impact Factor:8.075(SJIF)
Volume 5 | Special Issue 1 | 2025 Edition
National Level Conference on "Advanced Trends in Engineering Science & Technology" – Organized by RKCE

Five-Level Inverter for Renewable Power Generation System

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***Abstract*—In this paper, a five-level inverter is developed and applied for injecting the real power of the renewable power into the grid to reduce the switching power loss, harmonic distortion, and electromagnetic interference caused by the switching operation of power electronic devices. Two dc capacitors, a dual-buck converter, a full-bridge inverter, and a filter configure the five-level inverter. The input of the dual-buck converter is two dc capacitor voltage sources. The dual-buck converter converts two dc capacitor voltage sources to a dc output voltage with three levels and balances these two dc capacitor voltages. The output voltage of the dual-buck converter supplies to the full-bridge inverter. The power electronic switches of the full-bridge inverter are switched in low frequency synchronous with the utility voltage to convert the output voltage of the dual-buck converter to a five-level ac voltage. The output current of the five-level inverter is controlled to generate a sinusoidal current in phase with the utility voltage to inject into the grid. Simulation prototype is developed to verify the performance of the developed renewable power generation system. Simulation results show that the developed renewable power generation system reaches the expected performance.**

I. INTRODUCTION

The conventional single-phase inverter topologies for grid connection include half-bridge and full bridge[1]–[4].The half-bridge inverter is configured by one capacitor arm and one power electronic arm. The dc bus voltage of the half-bridge inverter must be higher than double of the peak voltage of the output ac voltage. The output ac voltage of the half-bridge inverter is two levels. The voltage jump of each switching is the dc bus voltage of the inverter. The full-bridge inverter is configured by two power electronic arms. The popular modulation strategies for the full-bridge inverter are bipolar modulation and unipolar modulation [3], [5]–[7]. The dc bus voltage of the full-bridge inverter must be higher than the peak voltage of the output ac voltage. The output ac voltage of the full-bridge inverter is two levels if the bipolar modulation is used and three levels if the unipolar modulation is used. The voltage jump of each switching is double the dc bus voltage of the inverter if the bipolar modulation is used, and it is the dc bus voltage of the inverter if the unipolar modulation is used. All power electronic switches operate in high switching frequency in both half-bridge and full Bridgein verters. The switching operation will resultins witching loss. The loss of power electronic switch includes the switching loss and the conduction loss. The conduction loss depends onthe handling power of power electronic switch. The switching loss is proportional to the switching frequency, voltage jump of each switching ,and the current of the power electronics witches. The power efficiency can be advanced if the switching loss of the dc–ac inverter is reduced. Multilevel inverter

can effectively reduce the voltage jump of each switching operation to reduce the switching loss and increase power efficiency. The number of power electronic switches used in the multilevel inverter is larger than that used in the conventional half-bridge and full-bridge inverters. Moreover, its control circuit is more complicated. Thus, both the performance and complexity should be considered in designing the multilevel inverter [8], [9]. However, interest in the multilevel inverter has been aroused due to its advantages of better power efficiency, lower switching harmonics, and a smaller filter inductor compared with the conventional half-bridge and full-bridge inverters. The conventional single-phase multilevel inverter topologies include the diode-clamped, the flying capacitor, and the cascade H-bridge types[10]–[15], as showninFig.1.Fig.1(a)shows the basic configuration of a diode-clamped multilevel inverter. As can be seen, it is configured by two dc capacitors, two diodes, and four power electronic switches. Two diodes are used to conduct the current loop, and four power electronic switches are used to control the voltage levels. The output voltage of the basic diode-clamped multilevel inverter has three levels. The voltage difference of each level is Vdc/2 (the voltage on a capacitor). Since the voltages of two dc capacitors are used to form the voltage level of the multilevel inverter, the voltages of these two dc capacitors must be controlled to be equal. The control for balancing these two dc capacitors is very important in controlling the diode-clamped multilevel inverter, and it isvery hard under the light load [16]–[19]. If the five-level output voltage is expected, extra two diodes and four power electronic switches are required [11], [20]. Fig. 1(b) shows the circuit configuration of a basic flying capacitor multilevel inverter. As can be seen, it is configured by three dc capacitors and four powe electronic switches. The voltage on each dc capacitor is controlled to be Vdc/2, and the output voltage of the basic flying capacitor multilevel inverter has three levels. The voltage difference of each level is also Vdc/2 (the voltage on a dc capacitor). These three dc capacitors must be controlled for maintaining their voltages to be Vdc/2 in the charge and discharge processes. Therefore, its control circuit is more complicated. If five-level output voltage is required, an extra dc capacitor and four power electronic switches are required [11], [13], [14]. Fig. 1(c) shows the circuit configuration of the basic cascade H-bridge multilevel inverter [8]–[11], [15], [21]. As can be seen, it is configured by two full-bridge inverters connected in cascade. The dc bus voltage of each full-bridge inverter is Vdc/2, and the output voltage of each full-bridge inverter can be controlled to be Vdc/2, 0, and −Vdc/2. Thus, the voltage levels of the output voltage of the cascade full-bridge multilevel inverter are Vdc,Vdc/2, 0, −Vdc/2, and −Vdc. This topology has advantages of fewer components being required compared with other multilevel inverters under the output voltage with the same levels, and its hardware circuit can be modularized because the configuration of each full bridge is the same. However, this topology has the disadvantages that two independent dc voltage sources are required. In this paper, a five-level inverter is developed and applied for injecting the real power of the renewable power into the grid. This five-level inverter is configured by two dc capacitors, a dual-buck converter, a full-bridge inverter, and a filter [22]. The five-level inverter generates an output voltage with five levels and applies in the output stage of the renewable power generation system to generate a sinusoidal current in phase with the utility voltage to inject into the grid. The power electronic switches of the dual-buck converter are switched in high frequency to generate a three-level voltage and balance the two input DC voltages. The power electronic switches of the full-bridge inverter are switched in low frequency synchronous with the utility to convert the output voltage of the dual-buck converter to a five-level ac voltage. Therefore, the switching power loss, harmonic distortion, and electromagnetic interference (EMI) caused by the switching operation of power electronic devices can be reduced, and the control circuit is simplified. Besides, the capacity of output filter can be reduced. A hardware prototype is developed to verify the performance of the developed renewable power generation system.

II. CIRCUIT CONFIGURATION

Fig. 2 shows the circuit configuration of the five-level inverter applied to a photovoltaic power generation system. As can be seen, it is configured by a solar cell array, a dc–dc converter, a five-level inverter, two switches, and a digital signal processor (DSP)-based controller. Switches SW1 and SW2 are placed between the five-level inverter and the utility, and they are used to disconnect the photovoltaic power generation system from the utility when islanding operation occurs. The load is placed between switches SW1 and SW2. The output of the solar cell array is connected to the input port of the dc–dc converter. The output port of the dc–dc converter is connected to the five-level inverter. The dc–dc converter is a boost converter, and it performs the functions of maximum power point tracking (MPPT) and boosting the output voltage of the solar cell array. This five-level inverter is configured by two dc capacitors, a dual buck converter, a full-bridge inverter, and a filter. The dual-buck converter is configured by two buck converters. The two dc capacitors perform as energy buffers between the dc–dc converter adhesive-level inverter. The output of the dual-buck converters connected to the full-bridge inverter to convert the dc voltage to ac voltage. An inductor is placed at the output of the full bridge inverter to form as a filter inductor for filtering out the high-frequency switching harmonic generated by the dual-buck converter.

III. OPERATION PRINCIPLE OF FIVE-LEVEL INVERTER

The operation of this five-level inverter can be divided into eight modes. Modes 1–4 are for the positive half-cycle, and modes 5–8 are for the negative half-cycle. Fig. 3 shows the operation mesophase-level inverter. As can be seen, the power electronic switches of the full-bridge inverter are switched in low frequency and synchronously with the utility voltage to convert the dc power into ac power for commutating. As seen in Fig. 3(a)–(d), the power electronic switches S4 and S7 are in the ON state, and the power electronic switches S5 and S6 are in the OFF state during the positive half-cycle. On the contrary, the power electronic switches S4 and S7 arenite OFF state, and the power electronic switches S5 and S6 are in the ON state during the negative half-cycle. Since the dc capacitor voltagesVC2 and VC3 are balanced by controlling the five-level inverter, the dc capacitor voltages VC2 and VC3 can be represented as follows:

$$VC2 = VC3 = 1/2Vdc. \quad (1)$$

The operation modes of this five-level inverter are stated as follows.

Mode 1: Fig. 3(a) shows the operation circuit of mode 1.The power electronic switch of the dual-buck converter S2 is turned ONandS3 is turned OFF. DC capacitor C2 is discharged through S2,S4, the filter inductor, the utility, S7, and D3 to form a loop. Both output voltages of the dual-buck converter and five-level inverter are Vdc/2.

Mode 2: Fig. 3(b) shows the operation circuit of mode 2.The power electronic switch of the dual-buck converter S2 is turned OFFandS3 isturnedON.DCcapacitorC3 is discharged through D2,S4,thefilter inductor, the utility, S7, and S3 to forma loop. Both output voltages of the dual-buck converter and five level inverters are Vdc/2.

Mode3:Fig.3(c)shows the operation circuit of mode 3. Both power electronic switches S2 and S3 of the dual-buck converter are turned OFF. The current of the filter inductor flows through the utility, S7,D3,D2, and S4. Both output voltages of the dual buck converter and five-level inverter are 0.

Mode4:Fig.3(d)shows the operation circuit of mode4.Bothpower electronic switches S2 and S3 of the dual-buck converter are turnedON.DCcapacitorsC2 andC3 are discharged together through

S2,S4, the filter inductor, the utility, S7, and S3 to form a loop. Both output voltages of the dual-buck converter and five-level inverter are Vdc.

Modes 5–8 are the operation modes for the negative halfcycle. The operations of the dual-buck converter under modes5–8 are similar to that under modes 1–4, and the dual-buck converter can also generate three voltage levels Vdc/2, Vdc/2, 0, and Vdc, respectively. However, the operation of the full-bridge inverter is the opposite. The power electronic switches S4 and S7 areinthe OFF state, andthepowerelectronicswitchesS5 and S6 are in the ON state during the negative half-cycle. Therefore, the output voltage of the five-level inverter for modes 5–8 will be −Vdc/2, −Vdc/2,0,and−Vdc, respectively. Considering operation modes 1–8, the full-bridge inverter converts the dc output voltage of the dual-buck converter with three levels to an ac output voltage with five levels which are Vdc,Vdc/2, 0, −Vdc/2, and −Vdc. The operation of power electronic switches S2 and S3 should guarantee the output voltage of the dual-buck converter is higher than the absolute of the utility voltage. The waveforms of output voltage of five-level inverter and utility voltage are shown inFig. 4.Due to the operation of full-bridge inverter, the voltage and current in the dc side of full-bridge inverter are their absolute values of the utility voltage and the output current of the fivelevel inverter. When the absolute of the utility voltage is smaller than Vdc/2, the output voltage of the dual-buck converter should change between Vdc/2and0.Accordingly, thepowerelectronicsof five-level inverter is switched between modes 1 or 2, and mode3duringthepositivehalf-cycle.On the contrary, the power electronics of five-level inverter is switched between modes 5 or 6, and mode 7 during the negative half-cycle. One of the power electronic switches S2 and S3 is in the OFFstate and the other is switched in high frequency during one PWM period. Fig. 5(a) shows the equivalent circuit for the dc side of the five-level inverter under |vs|<Vdc/2. As seen in Fig. 5(a), the equivalent circuit is a conventional buck converter. DC voltage source Vcx may be dc capacitor voltage VC2 or VC3, and it depends on which power electronic switch S2 or S3 is switching in high frequency. The change rate of the output current is negative, meaning the output current |io| will decrease when the power electronic switch is turned OFF. The output current |io| can be controlled by controlling the ON/OFF operation of the power electronics witch to track are Ference current signal. When the absolute of the utility voltage is higher than Vdc/2,the output voltage of the dual-buck converter should be changed between Vdc and Vdc/2. Accordingly, the five-level inverter is operated in mode 4, and 1 or 2 during the positive half-cycle, and it is switched in mode 8, and 5 or 6 during the negative half cycle. One of power electronic switches S2 and S3 is still turned ON and the other is switched in high frequency during one PWM period. Fig. 5(b) shows the equivalent circuit for the dc side of the five-level inverter under |vs| >Vdc/2. The dc voltage source Vdc is the summation of dc capacitor voltages VC2 and VC3. As seen in Fig. 5(b), it differs from the conventional buck converter, where voltage source VCx is connected to the diode in series. Voltage source Vcx may be dc capacitor voltage VC2 or VC3, and it depends on which power electronic switch S3 or S2 is switching in high frequency.

The change rate of the output current |io| is negative, and the output current |io| inductor current will be decreased when the power electronic switch is turned OFF. the output current |io| can also be controlled to track a reference current signal by controlling the ON/OFF operation of the power electronic switches under |vs| >Vdc/2. Hence, the output current of the five-level inverter can be controlled to track a reference current signal, which is a sinusoidal current in phase with the utility voltage by controlling the ON/OFF operation of the power electronic switches S2 and S3. Meanwhile, the five-level inverter will generate a five-level output voltage varying with the change of the utility voltage. The switching loss, filter inductor, and EMI are reduced because the voltage difference of each voltage level is only Vdc/2.

IV. VOLTAGE BALANCE OF FIVE-LEVEL INVERTER

Balancing the voltages of dc capacitors is very important in controlling the multilevel inverter. The voltage balance of dc capacitor voltages VC2 and VC3 can be controlled by the power electronic switches S2 and S3 easily. When the absolute of the utility voltage is smaller than Vdc/2, one power electronic switch either S2 or S3 is switched in high frequency and the other is still in the OFF state. Which power electronic switch is switched in high frequency depends on the dc capacitor voltages VC2 and VC3. If dc capacitor voltage VC2 is higher than dc capacitor voltage VC3, power electronic switch S2 is switched in high frequency. In this situation, the voltage source VCxin Fig. 5(a) is VC2, and C2 will be discharged. Thus, the dc capacitor voltages VC2 decreases and VC3 does not change. On the contrary, power electronic switch S3 is switched in high frequency when voltage VC3 is higher than voltage VC2. In this situation, the voltage source VCx in Fig. 5(a) is VC3. Thus, the dc capacitor voltagesVC3 decreases and VC2 does not change. In this way, the voltage balance of C2 and C3 can be achieved. When the absolute of the utility voltage is higher than Vdc/2, one power electronic switch either S2 or S3 is switched in high frequency and the other is still in the ON state. Which power electronic switch is switched in high frequency depends on the dc capacitor voltages VC2 and VC3. If dc capacitor voltage VC2 is higher than dc capacitor voltage VC3, the power electronic switch S3 is switch edin high frequency. The voltages ource in Fig. 5(b) is dc capacitor voltage VC2. When the power electronic switch S3 is turned ON, both C2 and C3 are discharged. However, onlyC2 supplies the power when the power electronic switch S3 is turned OFF. Thus, C2 will discharge more power than that of C3. On the contrary, the power electronic switch S2 is switched in high frequency when dc capacitor voltage VC3 is higher than dc capacitor voltage VC2. The voltage source VCx in Fig. 5(b) is dc capacitor voltage VC3. When the power electronic switch S2 is turned ON, both C2 and C3 are discharged. However,onlyC3 supplies the power when the power electronic switch S2 is turned OFF. Thus, C3 will discharge more power than that of C2. In this way, the voltage balance of C2 and C3 can be achieved. As mentioned earlier, the operation of power electronic switches S2 and S3 can be summarized as Table I. The voltages of capacitors C2 and C3 can be easily balanced compared with the conventional multilevel inverter.