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Newly-Constructed Simplified Single-Phase Multi-string Multilevel Inverter Topology for Distributed Energy Resources

R.Venkata Prasanna Govardhan[1], Donta Prudhvi[2], Golukonda Tharun[3], T. Srinivasa Rao[4]
[1,2,3,] UG Scholars, Department of Electrical and Electronics Engineering,
[4]Professor, Department of Electrical and Electronics Engineering,
[1,2,3,4]R K College of Engineering Vijayawada, India
[1]govardhanr2004@gmail.com

Abstract—In the microgrid system, the distributed energy resource (DER) based single-phase inverter is usually adopted. In order to reduce conversion losses, the key is to save costs and size by removing any kind of transformer as well as reducing the power devices. The objective of this paper is to study a novel five level multistring inverter topology for DERs based DC/AC conversion system. In this study, a high step-up converter is introduced as a front-end stage to improve the conversion efficiency of conventional boost converters and to stabilize the output DC voltage of various DERs such as PV and fuel cell modules for use with the simplified multilevel inverter. The simplified multilevel inverter requires only six active switches instead of the eight required in the conventional cascaded H bridge (CCHB) multilevel inverter. In addition, two active switches are operated under line frequency. The studied multistring inverter topology offers strong advantages such as improved output waveforms, smaller filter size, and lower EMI and THD. Simulation and experimental results show the effectiveness of the proposed solution.

I. INTRODUCTION

In light of public concern about global warming and climate change, much effort has been focused on development of environmentally friendly distributed energy resources (DERs). For delivering premium electric power in terms of high efficiency, reliability, and power quality, integrating interface converters of DERs such as photovoltaic, wind power, micro turbines, and fuel cells into the microgrid system has become a critical issue in recent years [1]-[4]. In such systems, most DERs usually supply a DC voltage that varies in a wide range according to various load conditions. Thus, a DC/AC power processing interface is required and is compliable with residential, industrial, and utility grid standards [4]-[7]. Various converter topologies have been developed for DERs [7]-[16] that demonstrate effective power flow control performance whether in grid-connected or stand-alone operation. Among them, solutions that employ high-frequency transformers or make no use of transformers at all have been investigated to reduce size, weight, and expense. For low medium power applications, international standards allow the use of grid-connected power converters without galvanic isolation, thus allowing so called " transformer less "architectures [7], [12]. Furthermore, as the output voltage level increases, the output harmonic content of such inverters decreases, allowing the use of smaller and less expensive output filters. As a result, various multilevel topologies are usually characterized by a strong reduction in switching voltages across power switches, allowing the reduction of switching power losses and electromagnetic interference (EMI) [8], [11]. A single-phase multistring five-level inverter integrated with an auxiliary circuit was recently proposed for DC/AC power conversion [12], [13]. This topology used in the power stage offers an important improvement in terms of lower component count and reduced output harmonics. Unfortunately, high switching losses in the additional auxiliary circuit caused the efficiency of the ***multistring five-level inverter to be approximately 4% less than that of the***

conventional multistring three-level inverter [13]. In [14], a novel isolated single-phase inverter with generalized zero vectors (GZV) modulation scheme was first presented to simplify the configuration. However, this circuit can still only operate in a limited voltage range for practical applications and suffer degradation in the overall efficiency as the duty cycle of the DC-side switch of the front-end conventional boost converter approaches unity [6], [14]. Furthermore, the use of isolated transformer with multi-windings of the GZV-based inverter results in the larger size, weight, and additional expense [14].

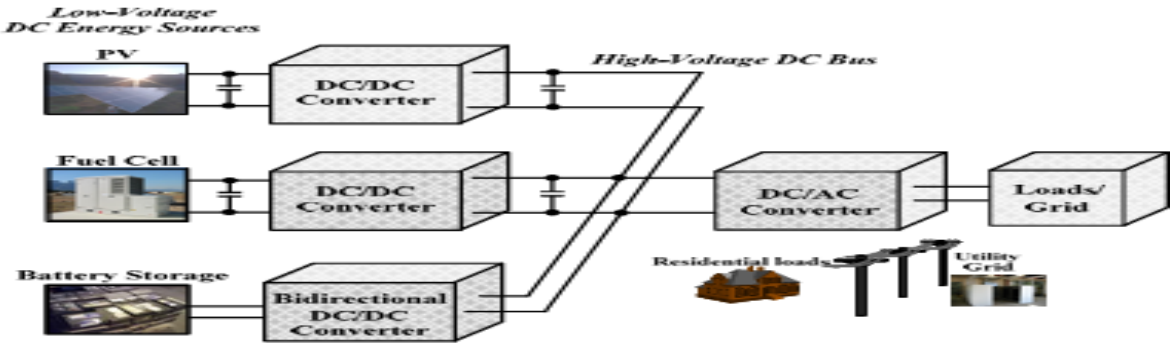

Fig. 1 Configuration of multistring inverter for various DERs application.

To overcome the above-mentioned problem, the objective of this paper is to study a newly-constructed transformerless five-level multistring inverter topology for DERs. In this paper, the foresaid GZV-based inverter is reduced to a multistring multilevel inverter topology that requires only six active switches instead of the eight required in the conventional cascaded H-bridge (CCHB) multilevel inverter [16]. In addition, among them, two active switches are operated under line frequency. In order to improve the conversion efficiency of conventional boost converters, a high step-up converter [26] is also introduced as a front-end stage to stabilize the output DC voltage of each DER modules for use with the simplified multilevel inverter. The newly-constructed inverter topology offer strong advantages such as improved output waveforms, smaller filter size, and lower EMI and total harmonics distortion (THD). In this paper, the operating principle of the developed system is described, and a prototype is constructed for verifying the effectiveness of the topology.

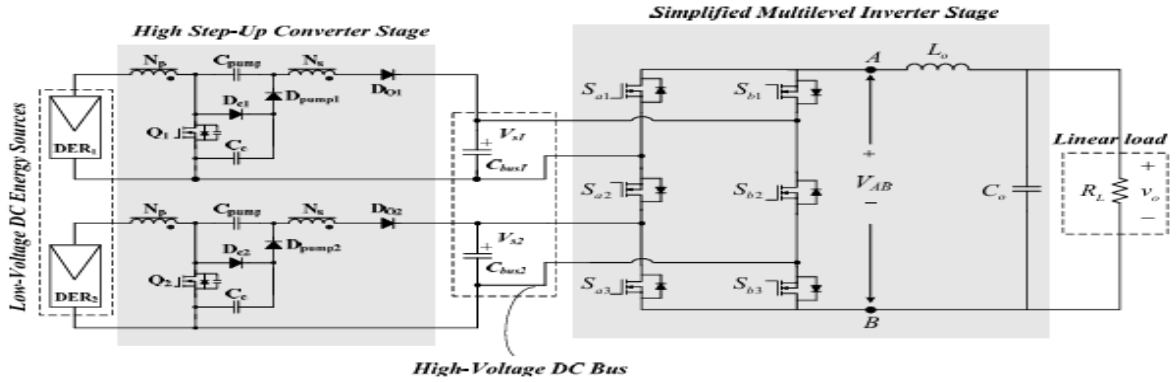

Fig. 2 Single-phase multistring five-level inverter topology.

II. SYSTEM CONFIGURATION OF OPERATION PRINCIPLES

A general overview of different types of photovoltaic (PV) modules or fuel cell inverters is given in [9] and [17]. This paper presents a multistring multilevel inverter for DERs application. The

multistring inverter shown in Fig. 1 is a further development of the string inverter, whereby several strings are interfaced with their own DC/DC converter to a common inverter [18]. This centralized system is beneficial because each string can be controlled individually. Thus, the operator may start his own PV/fuel cell power plant with a few modules. Further enlargements are easily achieved because a new string with a DC/DC converter can be plugged into the existing platform, enabling a flexible design with high efficiency [9]. The single-phase multistring multilevel inverter topology used in this study is shown in Fig. 2. This topology configuration consists of two high step-up DC/DC converters connected to their individual DC bus capacitor and a simplified multilevel inverter. Input sources, DER module 1, and DER module 2 are connected to the inverter followed a linear resistive load through the high step-up DC/DC converters. The studied simplified five-level inverter is used instead of a conventional phase disposition (PD) pulse width modulated (PWM) inverter because it offers strong advantages such as improved output waveforms, smaller filter size, and lower electromagnetic interference and THD [19]-[25]. It should be noted that, by using the independent voltage regulation control of the individual high step-up converter, voltage balance control for the two bus capacitors Cbus1, Cbus2 can be achieved naturally.

2.1 High Step-Up Converter Stage

In this study, high step-up converter topology in [26] is introduced to boost and stabilize the output DC voltage of various DERs such as PV and fuel cell modules for employment of the proposed simplified multilevel inverter. The architecture of a high step-up converter initially introduced from [26], depicted in Fig. 2, and is composed of different converter topologies: boost, flyback, and a charge pump circuit.

2.2 Simplified Multilevel Inverter Stage

To assist in solving problems caused by cumbersome power stages and complex control circuits for conventional multilevel inverters, this work reports a new single-phase multistring topology, presented as a new basic circuitry in Fig. 3. Referring to Fig. 2, it should be assumed that, in this configuration the two capacitors in the capacitive voltage divider are connected directly across the DC bus, and all switching combinations are activated in an output cycle. The dynamic voltage balance between the two capacitors is automatically controlled by the preceding high step-up converter stage. Then, we can assume Vs1=Vs2=Vs. This topology includes six power switches—two fewer than the CCHB inverter with eight power switches—which drastically reduces the power circuit complexity and simplifies modulator circuit design and implementation. The PD PWM control scheme is introduced to generate switching signals and to produce five output-voltage levels: zero, VS, 2VS, -VS, and 2VS.

This inverter topology uses two carrier signals and one reference to generate PWM signals for the switches. The modulation strategy and its implemented logic scheme in Fig. 4(a) and (b) are a widely used alternative for phase disposition modulation. With the exception of an offset value equivalent to the carrier signal amplitude, two comparators are used in this scheme with identical carrier signals Vtri1 and Vtri2 to provide high-frequency switching signals for switches Sa1, Sb1, Sa3 and Sb3. Another comparator is used for zero crossing detection to provide line-frequency switching signals for switches Sa2 and Sb2.

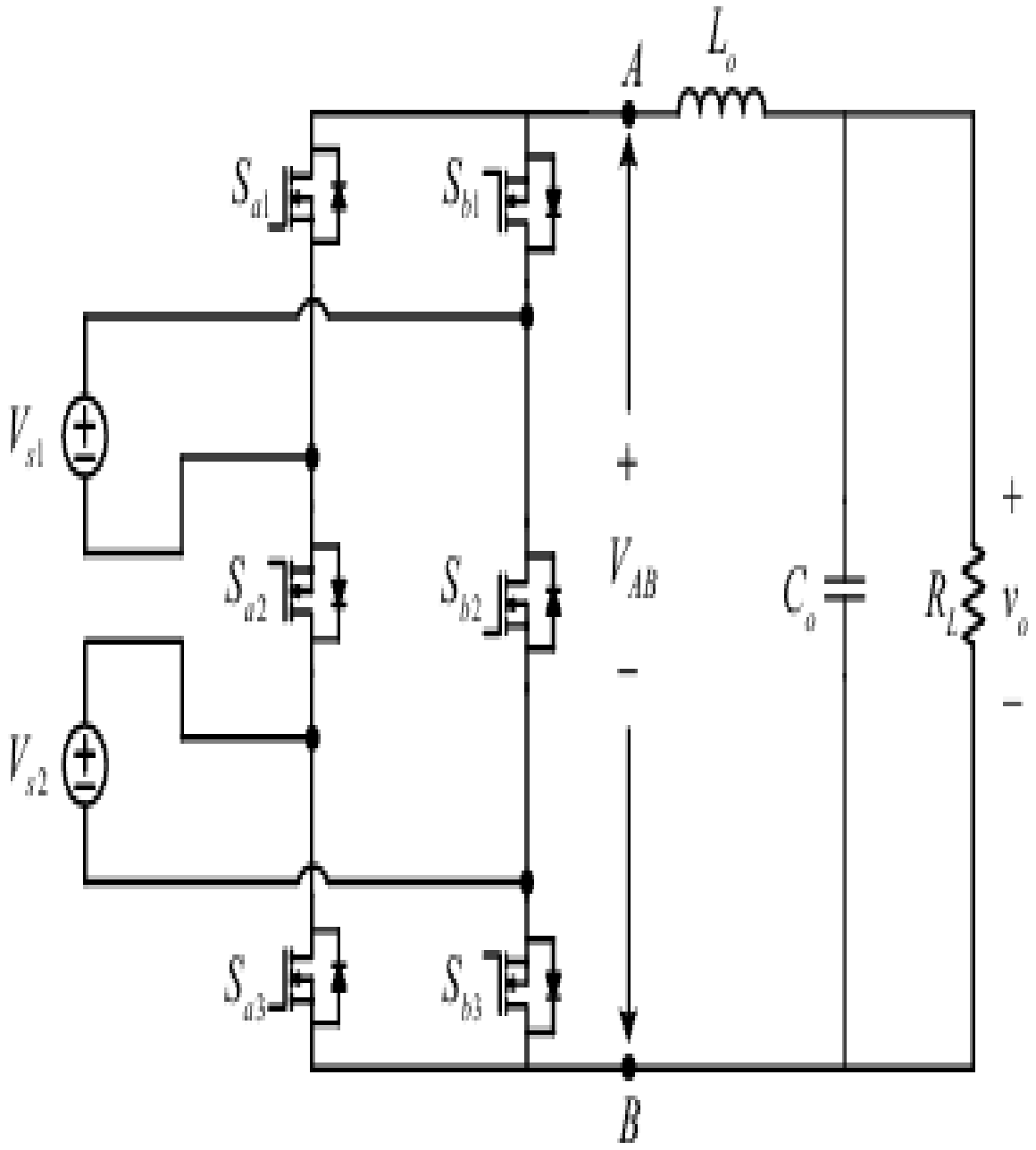

Fig. 3 Basic five-level inverter circuitry.

Table I. lists switching combinations that generate the required five output levels. The corresponding operation modes of the multilevel inverter stage are described clearly as follows:

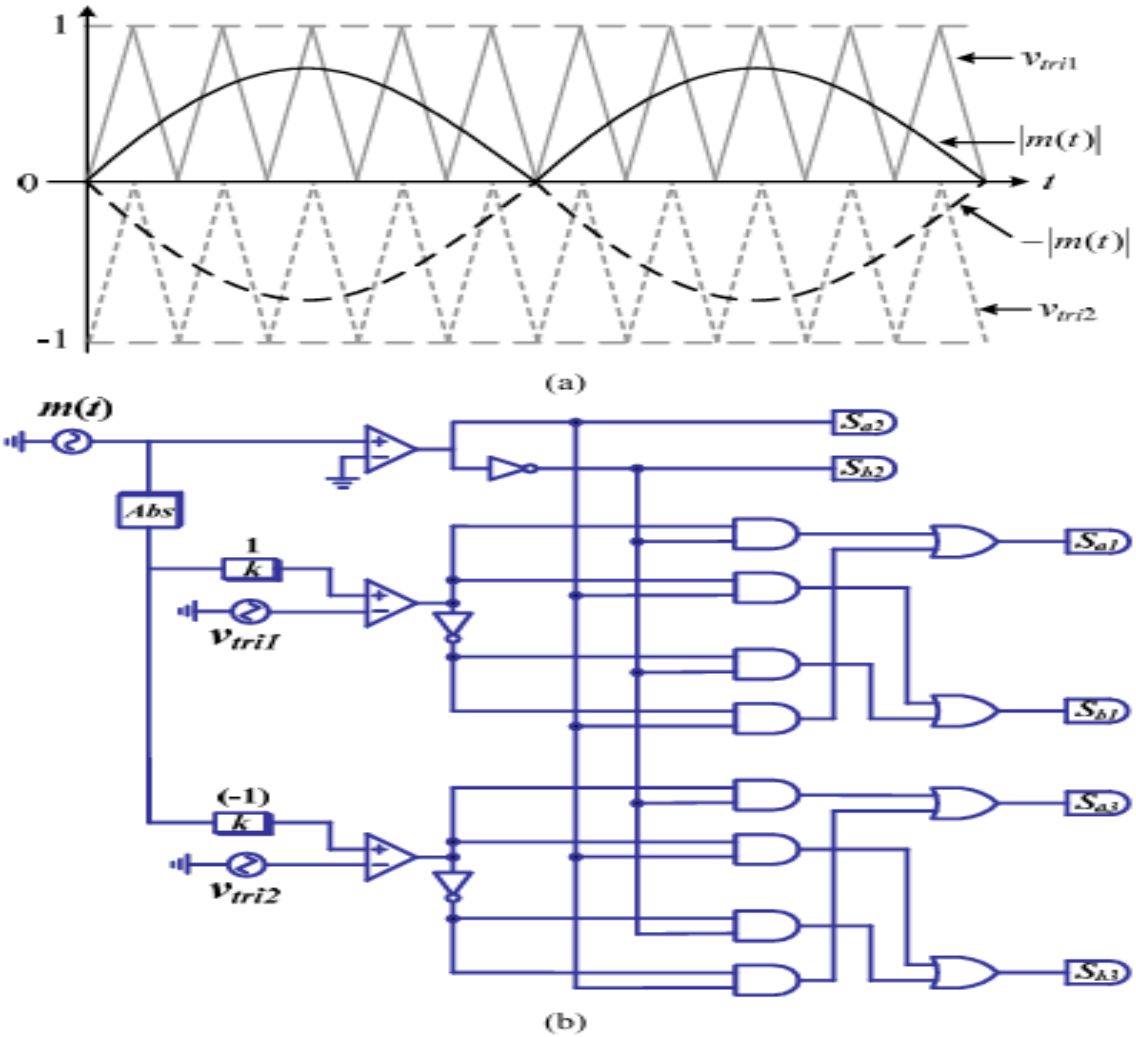

Fig. 4 Modulation strategy: (a) carrier/reference signals; (b) modulation logic.

(1) Maximum positive output, 2VS: Active switches Sa2, Sb1, and Sb3 are on; the voltage applied to the L-C output filter is 2VS. (2) Half-level positive output, +Vs: This output condition canbe induced by two different switching combinations. One switching combination is such that active switches Sa2, Sb1, Sa3 are on; the other is such that active switches Sa2, Sa1, Sb3 are on. During this operating stage, the voltage applied to the L-C output filter is +Vs. (3) Zero output, 0: This output condition can be formed by either of the two switching structures. Once the left or right switching leg is on, the load will be short-circuited, and the voltage applied to the load terminals is zero. (4) Half-level negative output, -Vs: This output condition can be induced by either of the two different switching combinations. One switching combination is such that active switches Sa1, Sb2, Sb3 are on; the other is such that active switches Sa3, Sb1, Sb2 are on. (5) Maximum negative output, -2Vs: During this stage, active switches Sa1, Sa3, and Sb2 are on, and the voltage applied to the L-C output filter is -2Vs. In the these operations, it can be observed that the open voltage stress of the active power switches Sa1, Sa3, Sb1, Sb3 are equal to input voltage VS; moreover, the main active switches Sa2 and Sb2 are operated at the line frequency.

Hence, the resulting switching losses of the new topology are reduced naturally, and the overall conversion efficiency is improved.

TABLE I.
SWITCHING COMBINATIONS

S_{a1}	S_{a2}	S_{a3}	S_{b1}	S_{b2}	S_{b3}	V_{AB}
0	1	0	1	0	1	$2V_S$
0	1	1	1	0	0	V_S
1	1	0	0	0	1	V_S
1	1	1	0	0	0	0
0	0	0	1	1	1	0
1	0	0	0	1	1	$-V_S$
0	0	1	1	1	0	$-V_S$
1	0	1	0	1	0	$-2V_S$

To verify the feasibility of the single-phase five-level inverter, a widely used software program PSIM is applied to simulate the circuit according to the previously mentioned operation principle. The control signal block is shown in Fig. 4; m(t) is the sinusoidal modulation signal. Both Vtri1 and Vtri2 are the two triangular carrier signals. The peak value and frequency of the sinusoidal modulation signal are given as mpeak=0.7 and fm=60Hz, respectively. The peak-to-peak value of the triangular modulation signal is equal to 1, and the switching frequency ftri1 and ftri2 are both given as 1.8kHz. The two input voltage sources feeding from the high step-up converter is controlled at 100V, i.e. Vs1=Vs2=100V. The simulated waveform of the phase voltage with five levels is shown in Fig. 5. The switch voltages of Sa1, Sa2, Sa3, Sb1, Sb2, and Sb3 are all shown in Fig. 6. It is evident that the voltage stresses of the switches Sa1, Sa3, Sb1, and Sb3 are all equal to 100V, and only the other two switches Sa2, Sb2 must be 200V voltage stress.

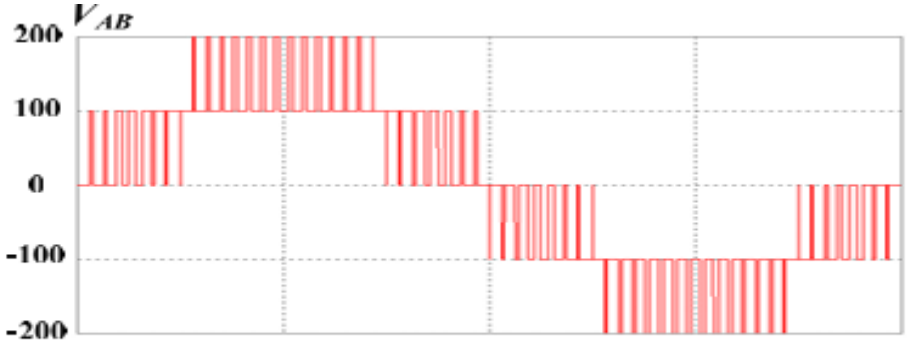

Fig. 5 Simulated waveforms of phase voltage V_{AB} of inverter stage [Scale: 100V/div]

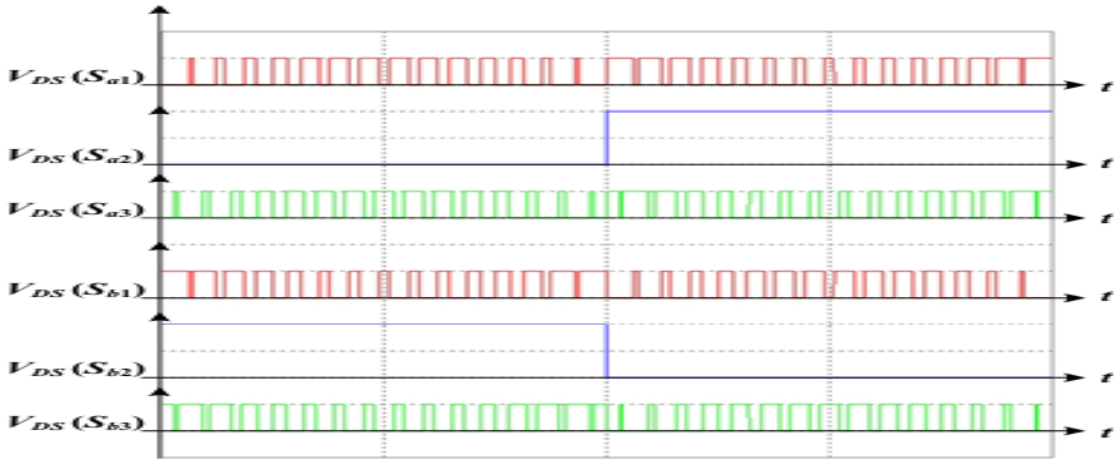

Fig. 6 Simulated waveforms of switch voltage for inverter stage within a line period. [Scale: 100V/div]

2.3. Comparison with CCHB inverter

Compared with the CCHB circuit topology as shown in Fig. 7, the voltage stresses of the eight switches of the CCHB inverter are all equal to Vs.

Because switches Sa2, Sb2 can only be activated twice in a line period (60Hz) and the switching frequency is larger than the line frequency (fs>>fm), the switching losses of the proposed circuit is approximated to 4Vsfs. Obviously, the switching power loss is nearly half that of the CCHB inverter.

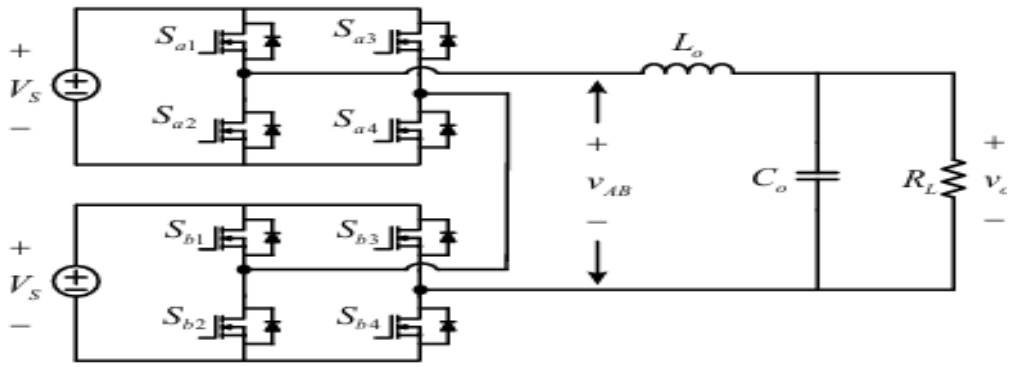

Fig. 7 Five-level inverter topologies of CCHB inverter [15].

Considering the harmonics in the inverter output voltage VAB, the amplitude of the fundamental and harmonic components in the output voltage VAB are calculated by PSIM software. The phase shift PWM technique is adopted for the CCHB Inverter. Both of the CCHB multilevel inverter and the studied multilevel inverter are operated in the same condition, including the same switching frequency 18kHz, the same modulation index ma ,the same input voltage VS=100V and output L-C filter, Lo=420uH, Co=4.7uF. Table II and Table III show the harmonic components and THD for the CCHB multilevel inverter and the studied multilevel inverter, respectively. It follows from Table II and Table III, one can find that the studied multilevel inverter have lower THD than the CCHB multilevel inverter. It implies that the output waveform is improved and smaller filter size can be used. Finally, for further revealing the potential merits of the studied multistring multilevel inverter, Table IV is provided to summarize

comparisons of the switch/diode number, voltage stress, switching losses for the CCHB multilevel inverter and the simplified single-phase five-level inverter.

TABLE II.
Harmonics of V_{AB} for CCHB Inverter

h	m_a=0.7	m_a=0.8
Fundamental 1	128.866V	150.984V
3	2.810V	2.780V
5	1.632V	1.604V
7	0.915V	0.981V
9	0.493V	0.573V
11	0.307V	0.301V
%THD V_{AB}	0.433	0.401
%THD v_o	0.020	0.018

Note: m_a is the modulation index; h is the harmonic order

TABLE III.
Harmonics of V_{AB} for New Multilevel Inverter

h	m_a=0.7	m_a=0.8
Fundamental 1	133.491V	155.605V
3	1.193V	1.250V
5	0.400V	0.492V
7	0.029V	0.131V
9	0.193V	0.076V
11	0.278V	0.169V
%THD V_{AB}	0.279	0.169
%THD v_o	0.009	0.008

TABLE IV.
COMPARISONS OF TWO MULTILEVEL INVERTERS

Inverter Type	CCHB Inverter	Studied Multilevel Inverter
Switch Numbers	8	6
Voltage Stress	$S_{a1} \sim S_{a4} : V_S$ $S_{b1} \sim S_{b4} : V_S$	$S_{a1}, S_{a3}, S_{b1}, S_{b3} : V_S$ $S_{a2}, S_{b2} : 2V_S$
Switching Loss	$P_{s,H-bridge} \propto 8V_s f_s$	$P_{s,proposed} \propto 4V_s f_s$
NOTES	(1) *CCHB Inverter*: All switches are operated with high frequency. (2) *New Multilevel Inverter*: S_{a2}, S_{b2} are operated under line frequency.	

III. EXPERIMENTAL RESULTS

To facilitate understanding of the operating principle and as verification, a prototype system with a high step-up DC/DC converter stage and the simplified multilevel DC/AC stage are built with the corresponding parameters listed in Table V. The specifications of the two preceding high step-up DC/DC converters are (a) input voltage 30V; (b) controlled output voltage 100V; and (c) switching frequency 85kHz. The corresponding specifications of the simplified multilevel DC/AC inverter stage are (1) output power, Po=230W; (2) input voltage, Vs=100V; (3) output voltage, vo=110Vrms; (4) line frequency, fm=60Hz; (5) switching frequency, fs=40kHz; and (6) peak modulation index, mpeak=0.76. For better understanding, the guidelines and considerations of the DC-link capacitance and the use of an L-C output filter at the output are described as follows.

3.1. Sizing DC-link capacitor

Figs. 8-9 show the PWM signals and voltage stresses of the six power switches for the five-level inverter, respectively. It is evident that the voltage stresses of the switches Sa1, Sa3, Sb1, and Sb3 are all equal to 100V, and only the other two switches Sa2, Sb2 must be 200V voltage stress. Fig. 10 shows steady state waveforms of output voltage vo, output current io, and the voltage applied to L-C output filter terminal VAB, respectively, for the inverter with a resistive load of 51Ω. As can be seen in Fig. 10, the waveform shows the desired five voltage levels: 200V, 100V, 0V, -100V, and -200V. The measured RMS value of vo is approximately 110V, while the measured RMS value of io is approximately 2.12A. The conversion efficiency of the implemented inverter and THD of the output voltage measured in this case are approximately 96% and 3%, respectively.

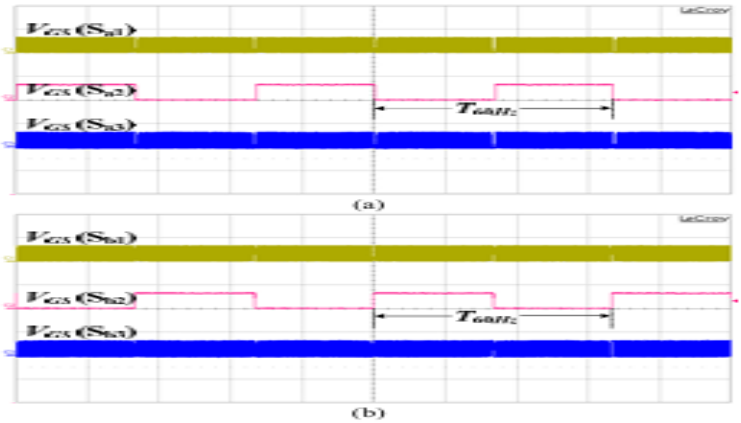

Fig. 8 Measured waveforms of PWM switching signals for inverter stage. [Scale: 10V/div, Time: 5ms/div]

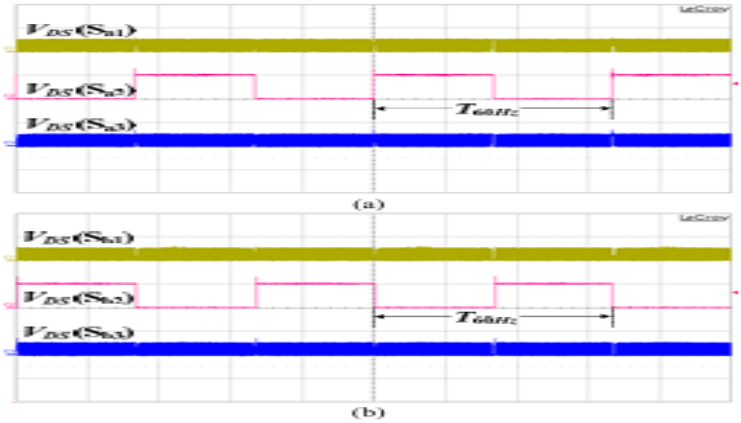

Fig. 9 Measured waveforms of voltage stresses of active switches for inverter stage. [Scale: 200V/div, Time: 5ms/div]

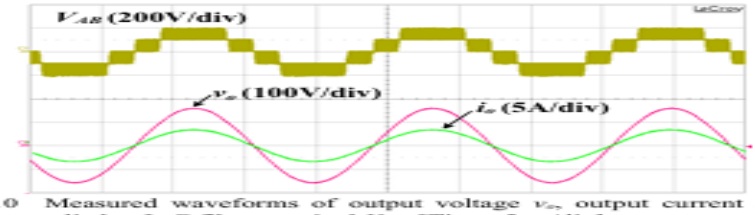

Fig. 10 Measured waveforms of output voltage v_o, output current i_o, and voltage applied to L-C filter terminal V_{AB}. [Time: 5ms/div]

IV. CONCLUSIONS

This work reports a newly-constructed single-phase multistring multilevel inverter topology that produces a significant reduction in the number of power devices required to implement multilevel output for DERs. The studied inverter topology offer strong advantages such as improved output waveforms, smaller filter size, and lower EMI and THD. Simulation and experimental results show the effectiveness of the proposed solution.

V.ACKNOWLEDGMENT

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VI.REFERENCES

[1] Y. Li, D. M. Vilathgamuwa, and P. C. Loh, "Design, analysis, and real time testing of a controller for multibus microgrid system," IEEE Trans. Power Electronics, vol. 19, no. 5, pp. 1195-1204, Sept. 2004.

[2] N. Hatziargyriou, H. Asano, R. Iravani, and C. Marnay, "Microgrids," IEEE Power and Energy Magazine, vol. 5, no. 4, pp. 78-94, Jul./Aug. 2007.

[3] F. Katiraei, R. Iravani, N. Hatziargyriou, and A. Dimeas, "Microgrids management," IEEE Power and Energy Magazine, vol. 6, no. 3, pp. 54 65, May/Jun., 2008

[4] C. L. Chen, Y. Wang, J. S. Lai, Y. S. Lee, and D. Martin, "Design of parallel inverters for smooth mode transfer microgrid applications," IEEE Trans. Power Electronics, vol. 25, no. 1, pp. 6-15, Jan. 2010.

[4] C. L. Chen, Y. Wang, J. S. Lai, Y. S. Lee, and D. Martin, "Design of parallel inverters for smooth mode transfer microgrid applications," IEEE Trans. Power Electronics, vol. 25, no. 1, pp. 6-15, Jan. 2010.

[6] C. T. Pan, C. M. Lai, and M. C. Cheng "A novel integrated single-phase inverter with an auxiliary step-up circuit for low-voltage alternative energy source application," IEEE Trans. Power Electronics, vol. 25, no. 9, pp. 2234-2241, Sep. 2010.

7] F. Blaabjerg, Z. Chen, and S. B. Kjaer, "Power electronics as efficient interface in dispersed power generation systems," IEEE Trans. Power Electronics, vol. 19, no. 5, pp. 1184-1194, Sep. 2004.

[8] D. G. Infield, P. Onions, A. D. Simmons, and G. A. Smith, "Power quality from multiple grid-connected single-phase inverters," IEEE Trans. Power Delivery, vol. 19, no. 4, pp. 1983-1989, Oct. 2004.

[9] N. A. Rahim and J. Selvaraj, "Multistring five-level inverter with novel PWM control scheme for PV application," IEEE Trans. Power Electronics, vol. 57, no. 6, pp. 2111-2123, Jun. 2010

[10] O. Lopez, R.Teodorescu, and J. Doval-Gandoy, "Multilevel transformerless topologies for single-phase grid-connected converters" IEEE Industrial Electronics Conference, pp. 5191-5196, 2006.