DESIGN AND ANALYSIS OF HIGH SPEED WALLACE TREE MULTIPLIER USING PARALLEL PREFIX ADDERS FOR VLSI CIRCUIT DESIGNS

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ABSTRACT:

Arithmetic and logic unit has been the most significant unit in any electronic devices. In the recent advancement, for an arithmetic and logic unit to be significant it needs to have an efficient algorithmic operation such as Multiplications and addition. Major operation block in any processing unit is a multiplier. There are many multiplication algorithms are proposed, by using which multiplier structure can be designed. Among various multiplication algorithms, Wallace tree multiplication algorithm is beneficial in terms of speed of operation. With the advancement of technology, demand for circuits with high speed and low area is increasing. In order to improve the speed of Wallace tree multiplier without degrading its area parameter, a new structure of Wallace tree multiplier is proposed in this paper. In the proposed structure, the final addition stage of partial products is performed by parallel prefix adders (PPAs). In this project, five Wallace tree multiplier structures are proposed using Kogge stone adder, Sklansky adder, Brent Kung adder, Ladner Fischer adder and Han carlson adder. Project will be developed using Verilog HDL. Xilinx ISE tool is used to perform the Simulation and Synthesis.

Keywords: Wallace tree multiplication algorithm, Kogge stone adder, Sklansky adder, parallel prefix adders (PPAs).

INTRODUCTION

In the process of evolution of technology, many Information Technology (IT) applications are requiring low-power integrated circuits (ICs), since handling huge amount of data to process. Due to integrated applications the size also increases. The energy efficiency is measured as the product of power consumption and computational time. To provide an energy efficient solution, the designer has to reduce the power consumption and the computing time as well. By reducing logic blocks, the static power can be reduced. However, reduction in power consumption has been achieved by different methods that demonstrates a trade-off relationship with circuit performance [1]. Low power consumption has become the decisive design goal in wide range of electronic systems and sub-systems. Inbuilt-powered sensing modules stand first in this row for the designers [2].

At present, the technology is advancing very rapidly in very short duration of time. The

circuits being design have some billions of components with low area, high speed and low power consumption. Hence area, speed and power plays crucial role in the design of any circuit [1], [2]. In order to satisfy the current trend demand a circuit must be designed with low area and less delay constraints. Arithmetic units are major blocks in any processing units which perform various arithmetic operations. Multiplication operation is important among all arithmetic operations. Several multiplication algorithms are studied in literature survey of multiplier designs like Binary multiplier, array multiplier, Booth's multiplier, Dadda multiplier, Wallace tree multiplier [4]. Wallace tree multiplier is advantageous in different types of multipliers[5].

LITERATURE SURVEY

Wallace Tree Multiplier Designs: A Performance Comparison Review by Himanshu Bansal, K. G. Sharma, Tripti Sharma

Multiplication process is often used in digital signal processing systems, microprocessors designs, communication systems, and other application specific integrated circuits. Multipliers are complex units and play an important role in deciding the overall area, speed and power consumption of digital designs. This paper presents a comparison review of various Wallace tree multiplier designs in terms of parameters like latency, complexity and power consumption.

Design of 64-bit low power parallel prefix VLSI adder for high speed arithmetic circuits by Nehru, K., A. Shanmugam, and S. Vadivel.

The addition of two binary numbers is the basic and most often used arithmetic operation on microprocessors, digital signal processors and data processing application specific integrated circuits. Parallel prefix adder is a general technique for speeding up binary addition. This method implements logic functions which determine whether groups of bits will generate or propagate a carry. The proposed 64-bit adder is designed using four different types prefix cell operators, even-dot cells, odd-dot cells, even-semi-dot cells and odd-semi-dot cells; it offers robust adder solutions typically used for low power and high-performance design application needs. The comparison can be made with various input ranges of Parallel Prefix adders in terms power, number of transistor, number of nodes. Tanner EDA tool was used for simulating the parallel prefix adder designs in the 250nm technologies.

A comprehensive review on the VLSI design performance of different Parallel Prefix Adders by Rakesh.S,K.S.Vijula Grace,

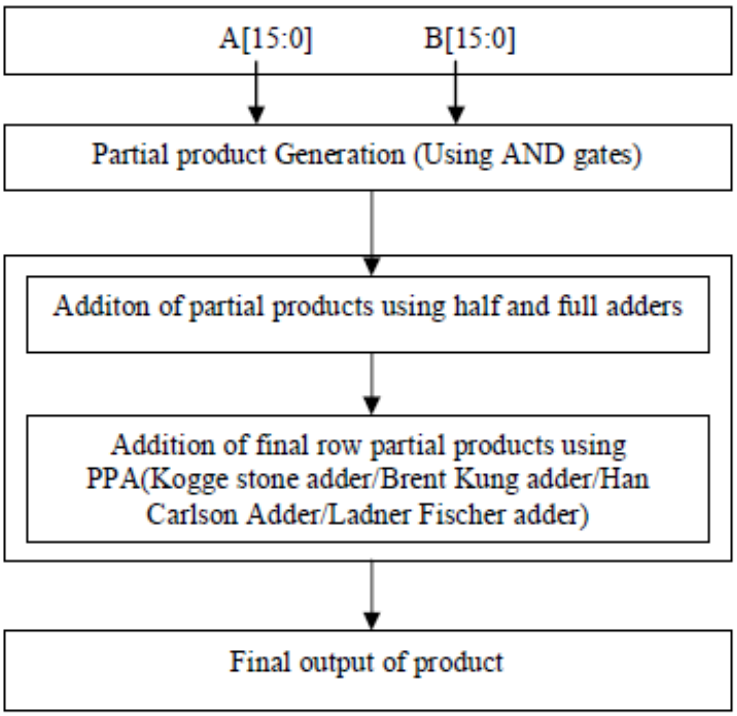
Adders are an important part of digital systems. In VLSI digital circuits, such adders should satisfy certain design constraints like low power and high speed. In this paper we present a review of the performance of some conventional adders and parallel adders. Parallel Prefix Adders (PPA) are considered to be one of the fastest adders that had been designed and developed. Parallel Prefix Adders were established as the most efficient circuits for binary addition. These adders which are also called Carry Tree Adders were found to have better performance in VLSI designs. This paper investigates the

performance of four different Parallel Prefix Adders namely Kogge Stone Adder (KSA), Brent Kung Adder (BKA), Han Carlson Adder (HCA) and Hybrid Han Carlson Adder (HHCA). In this paper the key contribution is the information about the structure of the Parallel Prefix Adders and their performance parameters. This paper can serve as a reference to the beginners in the digital electronics and VLSI area to gain more knowledge on the Carry Tree Adders.

PROPOSED SYSTEM

The Wallace tree multiplication process majorly has two phases. In phase 1, the input numbers are applied to AND gate to produce partial products. These partial products are added in step by step process by using half and full adders in phase 2 to obtain final product output. In detailed multiplication process of Wallace tree multiplier is explained through Fig.1 for input size of 4-bits. The phase 1 comprises of generation of partial products through multiplying every bit of given input numbers with each other. Four rows of partial products are generated as the size of input is 4- bits. The phase 2 comprises of many sub phases of addition of the partial products obtained in phase. The addition operation is carried out using half and full adders. Initially in phase 2, the addition operation is performed on first three rows of partial products generated in phase 1 which generates result of two rows having sum terms in first row and carry terms in second row. Then, the last row of partial products of phase 1 result is added with the sum and carry row which again result two rows comprising of one sum row and one carry row. To acquire final product, the sum and carry row are added. In this paper, Wallace tree multiplier structure is modified by using parallel prefix adders to add partial products in final phase addition process to obtain final product. The reason behind to use PPA in place of full adders is to improve the speed of operation. In PPA, the carry input for the next bits is generated at a time with the help of parallel prefix carry tree which consists of black cells and grey cells. There are many types of PPAs are present whose basic design idea is originated from carry look ahead adder. The PPA consists of three main blocks as shown in fig 2.

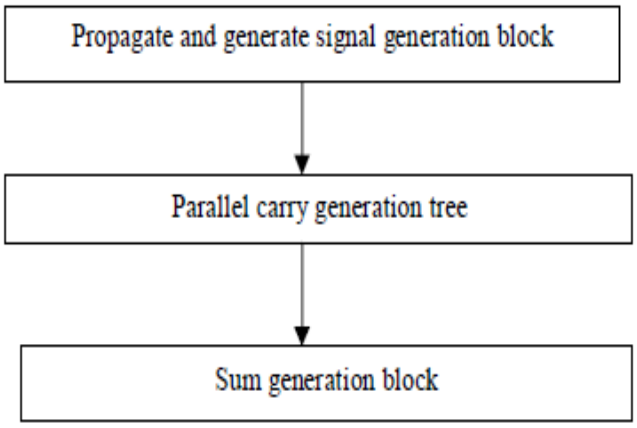
The multiplier operation is same which is performed in two phases as explained in section 2. In phase 1, partial products are generated with the help of AND gates. In Phase 2 partial products generated in phase 1 are added in step by step approach using half and full adders. In proposed design the final phase of addition of partial products in phase 2 is performed using PPA.



Block diagram of proposed Wallace tree multiplier using PPAs

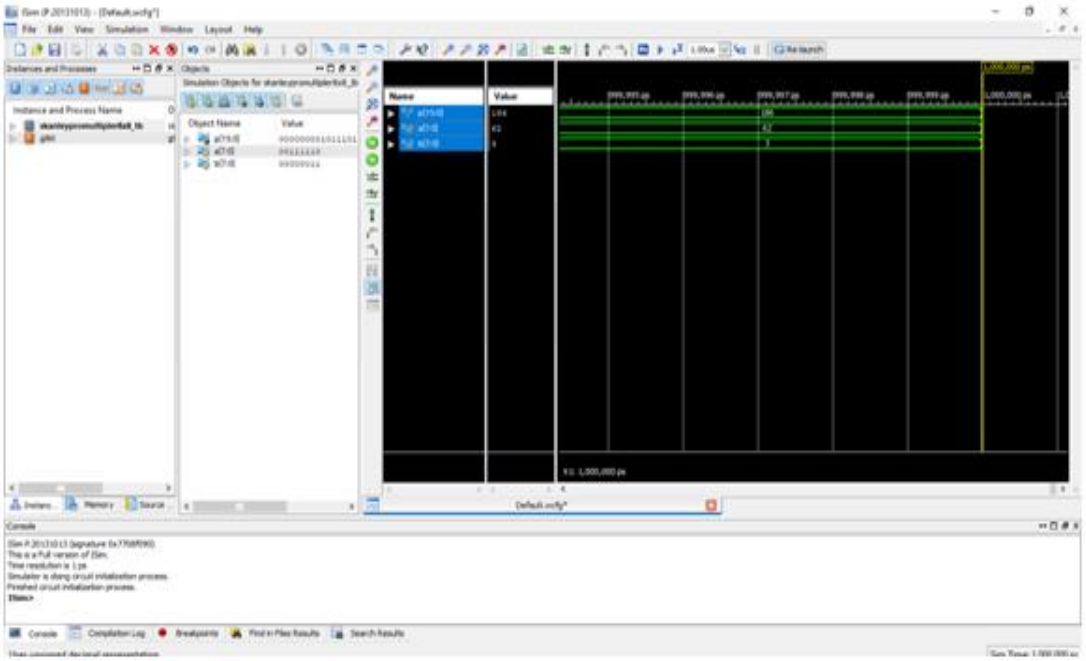
In the proposed multiplier, these last two rows are added with Kogge stone adder (KSA) [7] which is also known as a fast adder. Kogge Stone Adder (KSA) adds the bits in parallel prefix form as shown in Fig.2.

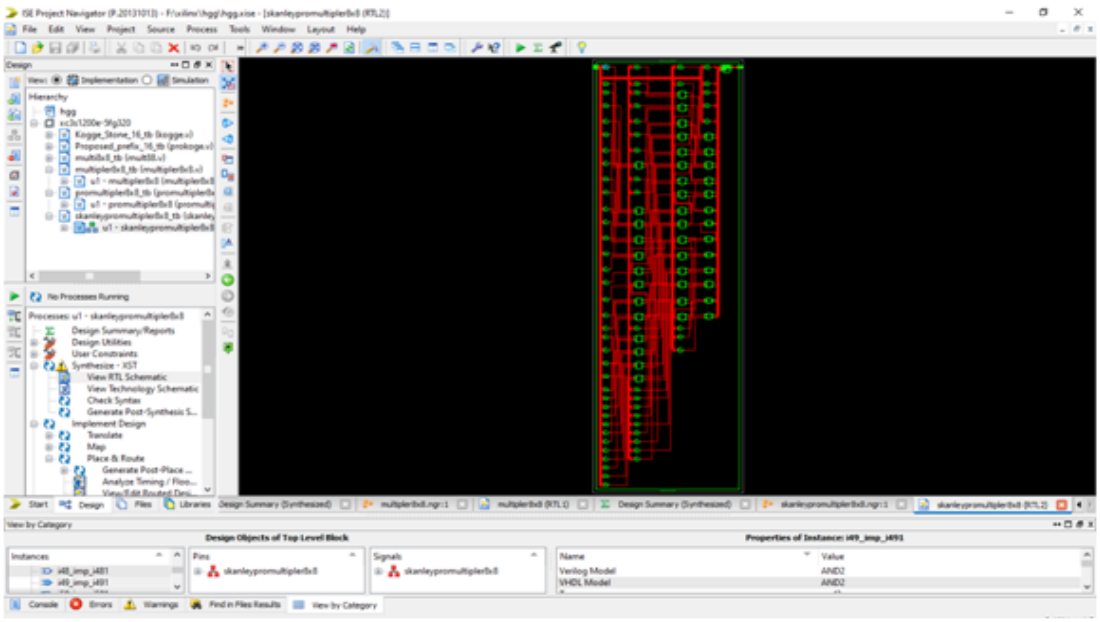
The Parallel Prefix expansion is done in three stages, which is appeared in fig1. The essential produce and engender sign are utilized to create the convey contribution for every adder. Two distinct administrators dark and dim are utilized here.



Addition procedure using Parallel Prefix tree structures

SIMULATION RESULTS





CONCLUSION

Total six multiplier structures are designed in this paper in which five are proposed Wallace tree multipliers using five different PPAs and one is traditional Wallace tree

multiplier. In terms of delay parameter it is achieved where as for area parameter the difference of LUTs occupied by traditional and proposed structures is not more which intend that area parameter is also achieved up to some extent which can be seen in table 1. In proposed multipliers, Wallace tree multiplier using Kogge stone adder is having least delay but its area parameter is high when compared to other structures of multipliers in this paper. In terms of area parameter, Wallace tree multiplier using Ladner fischer adder is having least area among proposed structures. So it can be concluded that the proposed multipliers are better in delay and area when compared with the traditional multiplier structure. Whereas for high speed application circuits, Wallace tree multiplier using Kogge stone adder can be used but costing little bit more area when compared to other proposed structures. The proposed multiplier structures can be used in high speed and low area application circuits basing on requirement. As future scope of this work, the multiplier structures can be designed by increasing input size(I.e. 32-bit,64- bit……). By designing the multiplier circuit with higher input size may lead to multiplier structure with less number of LUTs and also better delay value can be achieved.

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